CLAIMS

What is claimed is:

1. A digital programmable delay circuit with automatic calibration, comprising:

means for receiving a reference clock signal and providing a first output signal that is generated from the reference clock signal;

means for generating an oscillator signal, the means for generating an oscillator signal having a plurality of stages, one of the plurality of stages being programmable;

means for receiving the oscillator signal and providing a second output signal that is generated from the oscillator signal; and

means for receiving the first and second output signals and providing a third output signal based upon a relationship of the first and second output signals, the third output signal setting a delay of the programmable one of the plurality of stages.

2. The digital programmable delay circuit of Claim 1, wherein the means for generating an oscillator signal includes a means for enabling the generation of an oscillator signal.

3. The digital programmable delay circuit of Claim 1, wherein the means for receiving a reference clock signal has a first propagation delay and the means for receiving an oscillator signal has a second propagation delay, the first and second propagation delays being essentially identical.

4. The digital programmable delay circuit of Claim 3, wherein the means for receiving a reference clock signal includes a first counter and a first output logic circuit and the means for receiving an oscillator signal includes a second counter and a second output logic circuit.

5. The digital programmable delay circuit of Claim 4, wherein a number of stages of the first output logic circuit and a number of stages of the second output logic circuit are equal.

6. The digital programmable delay circuit of Claim 4, wherein a propagation delay of the first output logic circuit essentially equals a propagation delay of the second output logic circuit.

7. The digital programmable delay circuit of Claim 1, wherein the plurality of stages of the means for generating an oscillator signal is an odd number.

8. The digital programmable delay circuit of Claim 1, wherein the plurality of stages of the means for generating an oscillator signal is an even number.

9. A method for generating a delay, comprising:

entering a desired delay for an oscillator clock;

generating the oscillator clock from an oscillator;

generating a first signal in response to a reference clock;

generating a second signal in response to the oscillator clock;

comparing the first signal and the second signal; and

based on the comparison of the first and second signals and the desired delay, providing a programmable delay to the oscillator that is used to determine a frequency of the oscillator clock.

10. The method of Claim 9, wherein the oscillator is a ring oscillator.

11. The method of Claim 9, wherein the programmable delay is approximately 20 picoseconds.

12. The method of Claim 9, further comprising counting reference clock cycles as a first count value and generating the first signal through a Boolean operation using the first count value.

13. The method of Claim 12, further comprising counting oscillator clock cycles as a second count value and generating the second signal through a Boolean operation using the second count value.

14. The method of Claim 9, wherein the first and second signals are count values.

15. The method of Claim 14, wherein calibration and control logic compares the count values of the first and second signals to determine if the programmable delay is to be adjusted.

16. The method of Claim 15, wherein the method steps are repeated until the programmable delay is adjusted within desired parameters.

17. The method of Claim 16, further comprising disabling the oscillator clock.

18. The method of Claim 17, further comprising providing a source clock that is delayed by the programmable delay before providing a clock signal to a clock tree.

19. The method of Claim 18, wherein a portion of the clock tree forms part of the oscillator.

20. A programmable delay circuit with automatic calibration, comprising:

a calibration and control logic circuit that receives a first signal generated in response to a reference clock and a second signal generated in response to an oscillator clock; and

an oscillator circuit that generates the oscillator clock, the oscillator circuit including a programmable delay cell having a delay that is set by the calibration and control logic circuit.

21. The programmable delay circuit with automatic calibration of Claim 20, further comprising a first circuit that receives the reference clock and generates the first signal and a second circuit that receives the oscillator clock and generates the second signal.

22. The programmable delay circuit with automatic calibration of Claim 20, further comprising a first counting circuit that is timed by the reference clock and that generates the first signal.

23. The programmable delay circuit with automatic calibration of Claim 22, further comprising a second counting circuit that is timed by the oscillator clock and that generates the second signal.

24. The programmable delay circuit with automatic calibration of Claim 23, wherein the oscillator circuit includes a plurality of stages.

25. The programmable delay circuit with automatic calibration of Claim 24, wherein one of the plurality of stages is the programmable delay cell.

26. The programmable delay circuit with automatic calibration of Claim 24, wherein at least one of the plurality of stages is a complementary metal oxide semiconductor

inverter.

27. The programmable delay circuit with automatic calibration of Claim 24, wherein at least one of the plurality of stages is a differential delay cell.

28. A method for generating a delay, comprising:

enabling an oscillator circuit having a signal path;

setting a programmable delay in the signal path;

measuring a total delay in the signal path; and

adjusting the programmable delay to attain a desired total delay in the signal path.

29. The method of Claim 28, further comprising disabling the oscillator circuit.

30. The method of Claim 29, further comprising inputting another signal into the signal path.

31. The method of Claim 30, wherein at least a part of the signal path is part of a clock tree.

32. The method of Claim 30, wherein the another signal is a clock signal.